

## Brief Paper:

# Linearized Transistor Model Based Automated Biasing Scheme for Analog Integrated Circuits

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## Abstract

This work presents an automated transistor biasing scheme for analog integrated circuits. In order to effectively bias the transistor at a desired operating point, the proposed method uses a linearized transistor circuit model along with the curve fitted expressions obtained from the pre-simulated I-V characteristics of the actual transistor. As a result, the transistor size that leads to the desired operating point can be easily determined without heavily relying on the circuit simulator, which will lead to significant design time reduction. Furthermore, the proposed method is applied to an actual amplifier circuit where the design time based on the proposed biasing method showed 10× faster than the conventional design approach using the circuit simulator.

**Key Words:** Automated transistor biasing, Linearized transistor circuit model, Pre-simulated I-V data.

## I. INTRODUCTION

Analog integrated circuits are key hardware components for building new multi-media system applications including internet-of-things (IoT), 5G communication, and self-driving cars [1]. To comply with the emerging trends, new design methodologies for analog integrated circuits that can improve the circuit performance while maintaining good cost and power efficiency are in high demand [2]. Design automation is an ultimate goal for analog integrated circuits, since this can significantly improve the design time and productivity. However, unlike digital integrated circuits, where the design procedure can be fully automated – most of the digital processing algorithms realized using MATLAB codes or hardware description language (HDL) can be directly converted into transistor level circuits within several hours (this is called top-down design), analog circuits have a lot of limitations for design automation. This is mainly due to the non-linear behavior of the transistors that are used as basic elements.

A typical analog circuit design procedure consists of two major steps that are circuit topology selection and transistor biasing. In case of MOS transistors, biasing is setting the transistor size, in other words the aspect ratio (W/L) where W and L are the width and length, and fixing the operating voltages including the gate-to-source voltage

$V_{GS}$  and drain-to-source voltage  $V_{DS}$ , and the current  $I_D$  so that the transistor properly operates in the desired operation region [3]. However, due to the non-linear current-voltage (I-V) characteristics of the transistor, transistor biasing heavily rely on the case-by-case experience of the circuit designer and the circuit simulator, which is not very systematic and time consuming.

In this work, in order to overcome the limitations of analog integrated circuit design, in particular reducing the design time, a transistor circuit model based design method that can represent the saturation region operation with linear circuit components is proposed. This is similar to the linear circuit model used for time-mode circuits [4] and image processing circuits [5], however the proposed model is more specialized for MOS transistors. Since the proposed design method can replace the non-linear transistor with a linear circuit model, biasing will be simple and straightforward compared to the conventional design method that deals with the transistor as it is. As a result, the proposed design method can systematically bias the transistors without heavily relying on the designer's experience and the circuit simulator, which will reduce the design time as well. However, the proposed biasing scheme differs from the well-known  $g_m/I_D$  method which also use charts and tables obtained from pre-simulated transistor data, since the main objective of  $g_m/I_D$  is to optimize the

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circuit performance and power consumption instead of biasing the transistor [6]. In order to verify the proposed method, a single-ended folded cascode amplifier will be used as a biasing example, where the transistor sizes are set so that the desired operating point is achieved without using the circuit simulator.

## II. AUTOMATED BIASING SCHEME

This section will describe the automated transistor biasing method based on linearized transistor circuit model, where an actual amplifier circuit will be used as an example to verify the effectiveness of the proposed biasing scheme.

### 2.1. Biasing example

Fig. 1 shows the single-ended folded cascode amplifier that will be used as the biasing example. This amplifier circuit is widely used in a variety of applications including IoT [7]. Table 1 shows the design constraint where the  $W$  of each transistor will be set based on the proposed biasing method such that the transistors operate at the desired DC bias point ( $V_{DS}$  and  $V_{GS}$ ). However, before biasing the transistors, in order to satisfy all the other design constraints, the value of  $I_{ss}$ ,  $V_{B1}$ ,  $V_{B2}$ ,  $V_{B3}$ , and  $R_D$  should be determined.

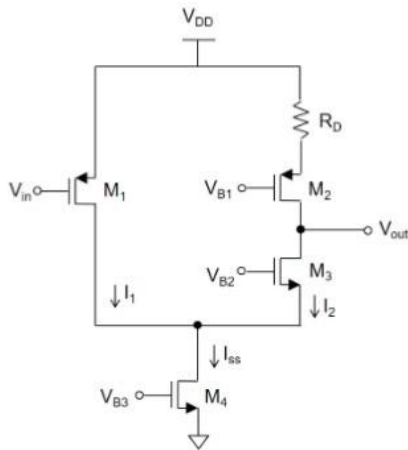


Fig. 1. Single-ended folded cascode amplifier.

Table 1. Single-ended folded cascode amplifier design constraints.

Parameter	Value
Trans-conductance ( $g_m$ )	$\geq 350\mu A/V$
Power consumption ( $P_D$ )	$\leq 480\mu W$
Supply voltage ( $V_{DD}$ )	3V
Threshold voltage ( $V_{TH}$ )	0.59V (nmos), -0.75V (pmos)
$V_{GS}$	1V (nmos), 0.9V (pmos)
$V_{DS}$	$ V_{DS1}  = 2V$ , $ V_{DS2}  = 0.6V$ , $V_{DS3} = 0.5V$ , $V_{DS4} = 1V$
$W, L$	$L = 1\mu m$ , $0.5\mu m \leq W \leq 10\mu m$

The steering current  $I_{ss}$  is bounded by the power consumption  $P_D$  and the trans-conductance  $g_m$  which are given as

$$P_D = I_{ss} \cdot V_{DD} \quad (1)$$

$$g_m = \frac{2I_1}{V_{ov1}} \quad (2)$$

where  $V_{ov1} = V_{GS1} - V_{TH}$  and  $I_1 = I_{ss}/2$ , since  $I_1 = I_2$  and  $I_{ss} = I_1 + I_2$ . As a result,  $I_{ss}$  is set to the smallest possible value 54uA. Next, the input common mode voltage  $V_{I,cm}$  and the fixed DC gate bias  $V_{B1}$ ,  $V_{B2}$ , and  $V_{B3}$  are set based on the  $V_{DS}$  and  $V_{GS}$  requirement of each transistor.  $V_{I,cm}$  is set by  $V_{DD}$  and  $V_{GS1}$ . That is,

$$V_{I,cm} = V_{DD} - |V_{GS1}|. \quad (3)$$

$V_{B1}$  is obtained from the following relationship

$$V_{B1} = V_{DS4} + V_{DS3} + |V_{DS2}| - |V_{GS2}|. \quad (4)$$

Since the source of  $M_4$  is tied to GND,  $V_{B2}$  is given as

$$V_{B2} = V_{GS3} + V_{DS4}. \quad (5)$$

The gate bias voltages that satisfy the  $V_{DS}$  and  $V_{GS}$  requirement for each transistor are  $V_{I,cm} = 2.1V$ ,  $V_{B1} = 1.2V$ ,  $V_{B2} = 2V$ , and  $V_{B3} = 1V$ . Also, the value of  $R_D$  is obtained by

$$R_D = \frac{V_{DD} - V_{s2}}{I_2}, \quad (6)$$

where  $V_{s2}$  is the source voltage of  $M_2$  which is given as

$$V_{s2} = |V_{DS2}| + V_{DS3} + V_{DS4}. \quad (7)$$

As a result, the value of  $R_D$  that meets the design constraint is 33.6k $\Omega$ .

### 2.2. Linearized transistor circuit model

The proposed transistor circuit model is a linear model that represents the strong inversion saturation region operation of the transistor, since most of the analog circuits are realized based on the saturation region operation. Fig. 2(a) shows the nmos transistor symbol, (b) the proposed circuit model, and (c) the I-V curve that shows the two operation regions. Depending on the value of  $V_{DS}$ , the operation region of the transistor can be divided into two regions - linear ( $V_{DS} < V_{ov}$ ) and saturation ( $V_{DS} > V_{ov}$ ) where  $V_{ov}$  is the boundary voltage that is equivalent to  $(V_{GS} - V_{TH})$  where  $V_{TH}$  is the threshold voltage. Although the transistor is a non-linear device, the saturation region can be modeled with simple circuit components such as the current/voltage source and the resistor, since the saturation region current  $I_D$  has a linear relationship with  $V_{DS}$ . Therefore, the key ideal of the proposed transistor circuit model is to divide  $I_D$  into two components that are the active current  $I_A$  and the passive current  $I_p$ , which is represented by the left and right branch in the circuit model. In addition,

$I_A$  depends on  $V_{GS}$  and  $I_P$  is determined by  $V_{DS}$ ,  $R_{out}$ , and  $V_{ov}$  where  $R_{out}$  is the saturation region output resistance. The expressions for  $I_A$  and  $I_P$  of the nmos are given as

$$I_A = \left(\frac{1}{2}\right) \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2, \quad (8a)$$

$$I_P = \frac{V_{DS} - V_{ov}}{R_{out,n}}. \quad (8b)$$

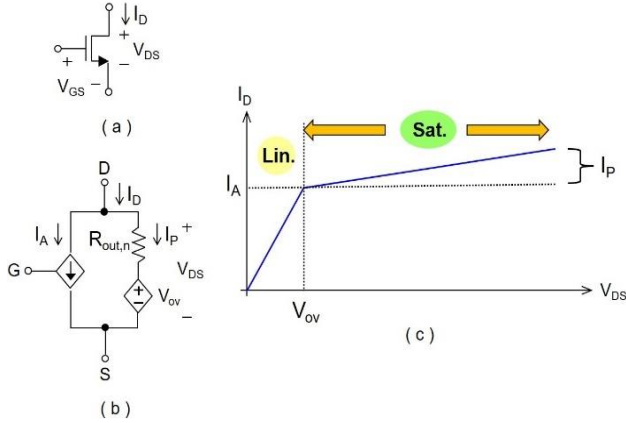


Fig. 2. (a) nmos transistor symbol. (b) linearized transistor circuit model. (c) I-V characteristic.

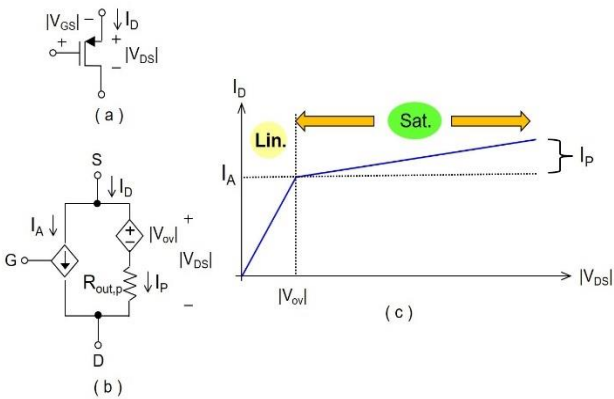


Fig. 3. (a) pmos transistor symbol. (b) linearized transistor circuit model. (c) I-V characteristic.

Fig. 3(a) shows the pmos transistor symbol. (b) the proposed circuit model, and (c) the I-V curve, where the circuit model is similar to the NMOS, except  $V_{GS}$ ,  $V_{DS}$ ,  $V_{ov}$ , and  $V_{TH}$  are negative, and the electron mobility  $\mu_n$  will be replaced with hole mobility  $\mu_p$ . The expressions for  $I_A$  and  $I_P$  of the pmos are given as

$$I_A = \left(\frac{1}{2}\right) \mu_p C_{ox} \left(\frac{W}{L}\right) (|V_{GS}| - |V_{TH}|)^2, \quad (9a)$$

$$I_P = \frac{|V_{DS}| - |V_{ov}|}{R_{out,p}}. \quad (9b)$$

### 2.3. Proposed transistor biasing method

Once the  $V_{DS}$ ,  $V_{GS}$ , and  $I_D$  of the transistors are determined, each transistor in the amplifier circuit will be replaced with the linearized transistor circuit model where

$W$  of the transistors are set based on the desired operating point – this is the biasing procedure. Toward this end, we will first find the passive current  $I_P$  based on eq. (8b) and (9b), and find the active current  $I_A$  using

$$I_A = I_D - I_P \quad (10)$$

However, to avoid heavily relying on the circuit simulator, curve fitted expressions obtained from the pre-simulated data of  $R_{out}$  and  $I_A$  will be used for finding  $I_P$  and  $W$  of each transistor. The pre-simulation data is obtained using Cadence Spectra mixed signal circuit simulator.

Fig. 4(a) and (b) show  $R_{out}$  vs.  $I_D$  for the nmos and pmos, where the dots indicate the pre-simulation data and the red line is the curve fitted plot obtained from power fit. The curve fitted expression for the nmos and pmos are given as

$$R_{out,n}(I_D) \approx 91.99 I_D^{-0.8259} + 2.079 \times 10^5 \quad (11a)$$

$$R_{out,p}(I_D) \approx 91.11 I_D^{-0.8133} + 7.987 \times 10^5 \quad (11b)$$

Using the above expressions,  $R_{out}$  at the desired bias current  $I_D$  can be obtained, where for  $M_1, M_2, M_3$ ,  $I_D = I_{ss}/2$  and for  $M_4$ ,  $I_D = I_{ss}$ . In addition, Fig. 5(a) and (b) show  $I_A$  vs.  $W$  of the nmos ( $V_{GS} = 1V$ ) and pmos ( $|V_{GS}| = 0.9V$ ), where the dots indicate the pre-simulated data and the red line is the curved fitted plot obtained from linear fit. The curve fitted expressions for the nmos and pmos are given as:

$$I_{A,n}(W) \approx 16.32W - 5.971 \times 10^{-8}. \quad (12a)$$

$$I_{A,p}(W) \approx 7.129W - 1.709 \times 10^{-6}. \quad (12b)$$

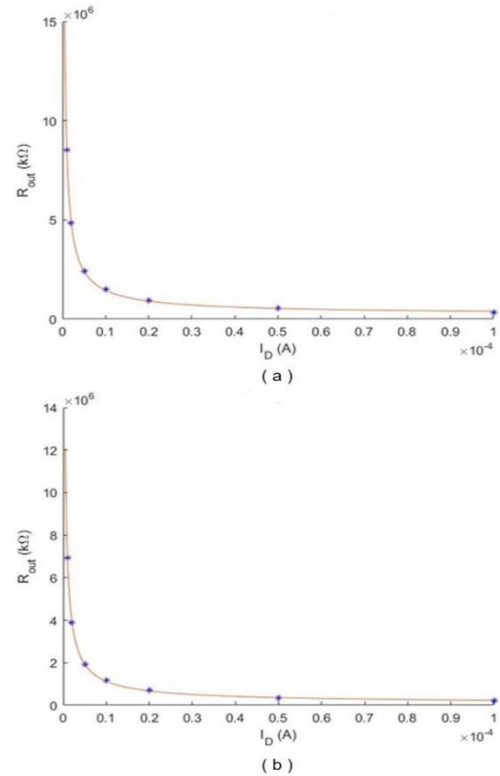


Fig. 4.  $R_{out}$  vs.  $I_D$  (a) nmos. (b) pmos.

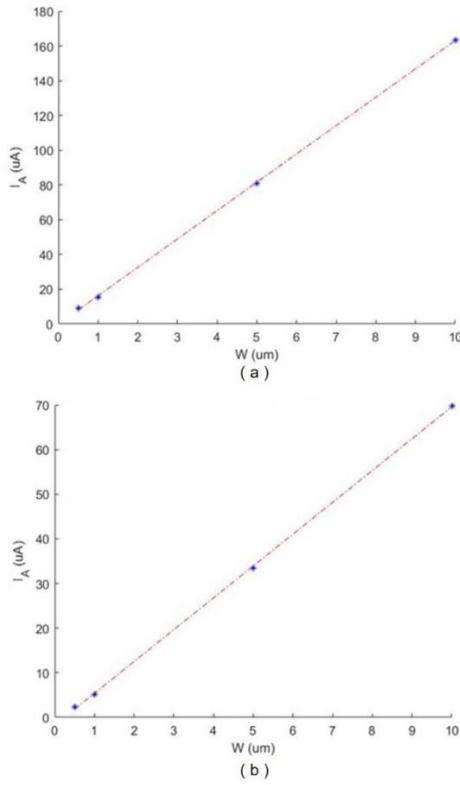


Fig. 5.  $I_A$  vs.  $W$  (a) nmos,  $V_{GS} = 1V$ . (b) pmos,  $|V_{GS}| = 0.9V$ .

Based on the above expressions,  $W$  corresponding to  $I_A$  can be obtained. This  $W$  will enable the transistor to operate at the desired  $V_{DS}$ ,  $V_{GS}$ , and  $I_D$ . Table 2 shows the  $R_{out}$ ,  $I_P$ ,  $I_A$ , and  $W$  of each transistor obtained from the proposed biasing method, where a MATLAB program is used to compute  $R_{out}$ ,  $I_P$ ,  $I_A$ , and  $W$ . As shown, the proposed biasing method only use basic pre-simulation data for the nmos and pmos instead of heavily relying on the circuit simulator throughout the entire biasing steps, which can enable a faster design time. Furthermore, to show the effectiveness of the proposed biasing scheme, the same single-ended folded cascode amplifier (Fig. 1) has been biased with the conventional approach (mainly using the circuit simulator), where design (biasing) time of the proposed method showed  $10\times$  faster than the conventional method.

Table 2. Biasing results obtained from the proposed method.

Transistor	$R_{out}$ (k $\Omega$ )	$I_P$ (uA)	$I_A$ (uA)	$W$ (um)
M <sub>1</sub>	548	3.37	23.63	3.61
M <sub>2</sub>	548	0.82	26.18	3.98
M <sub>3</sub>	754	0.13	26.87	1.65
M <sub>4</sub>	516	1.16	52.84	3.30

### III. CONCLUSION

This work presents an automated transistor biasing scheme for analog integrated circuits based on the linearized transistor circuit model along with the curve fitted expressions obtained from the pre-simulated I-V characteristics of the transistor. As a result, the transistor size that leads to the desired operating point can be easily determined without heavily relying on the circuit simulator, which leads to significant design time reduction. The proposed method is applied to an actual amplifier circuit where the design time based on the proposed biasing method showed  $10\times$  faster than the conventional design approach using the circuit simulator. As a future work, the proposed method will be applied to biasing different types of amplifiers.

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